HyperTransport™ Technology

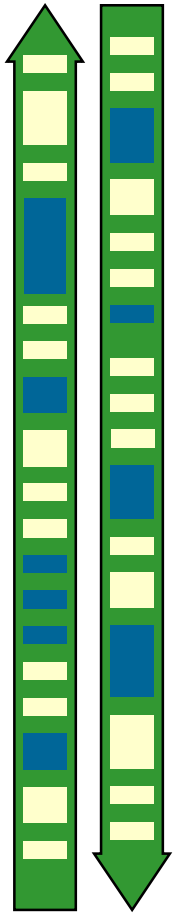
February 2001

AMD Technological Innovation

- **AMD Athlon™ Processor**
  - Industry's first seventh-generation architecture
- **AMD-760™ chipset**
  - Created the first commercially available platform supporting next-generation DDR memory technology
- **AMD PowerNow!™ technology**
  - Smart battery saving invention
- **x86-64 technology**
  - Seamless migration path to 64-bit computing
- **HyperTransport™ technology**
  - Moving information faster

HyperTransport™ Technology
Moving Information Faster

- **Innovative, high-speed chip-to-chip system link**
  - Packet-based technology
  - Connections have two unidirectional point-to-point links with varied bit widths
  - Allows multiple devices to be daisy chained
- **Designed to reduce data bottlenecks**
  - Allows system designers to move slower devices out of critical information paths
  - Designed to work in concert with existing devices as well as next-generation input or output components
- **Designed to allow information to move throughout an entire system faster**
  - Designed to allow components to communicate up to 24 times faster than with current technologies
  - Designed to enable a peak data transfer rate of 6.4GB/sec
- **Enables new performance levels for systems that power the Internet**
  - Computers
  - Networking Equipment
  - Communication Devices



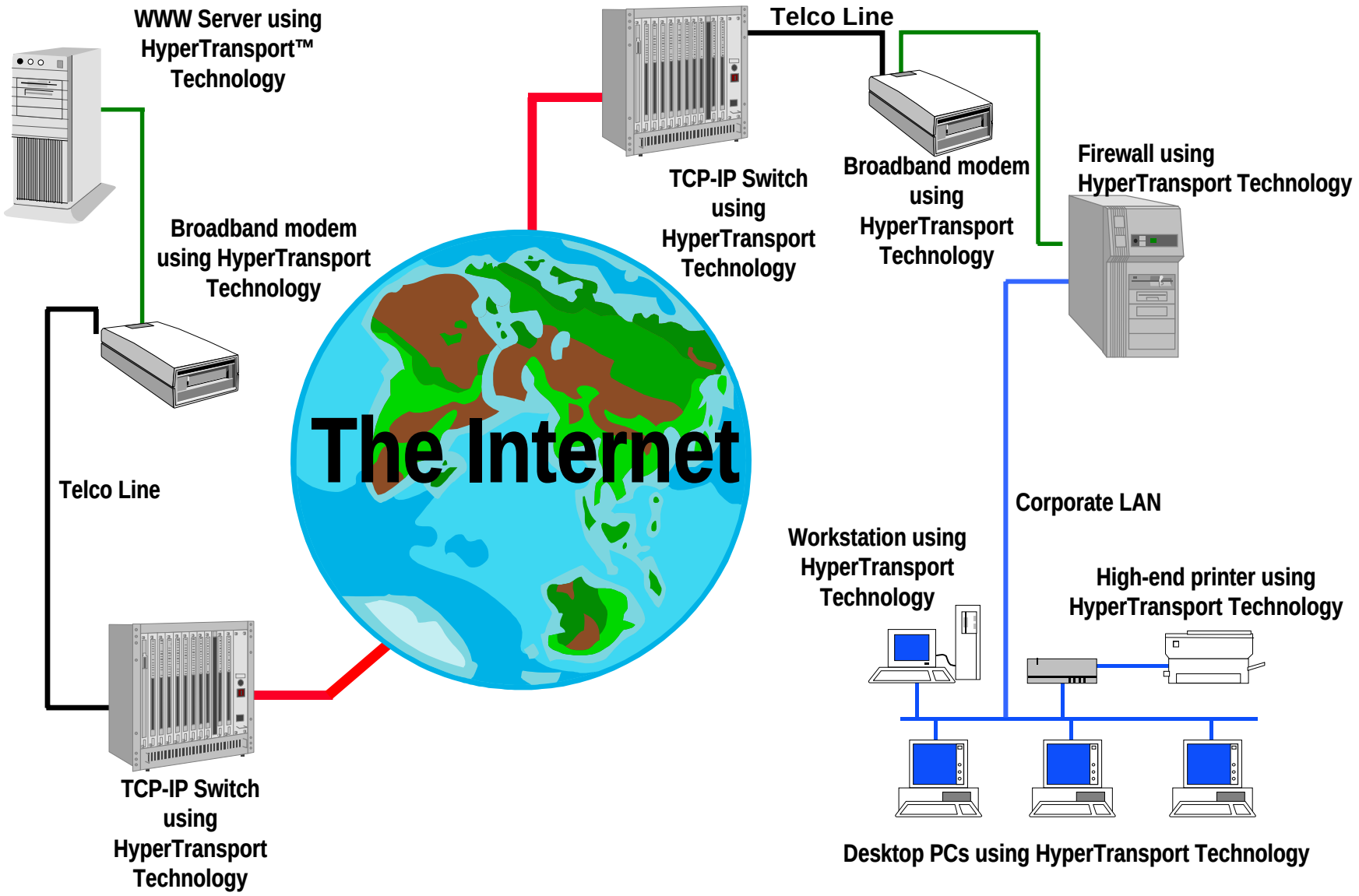
HyperTransport™ Partners

- **HyperTransport™ technology has widespread support throughout the computer and communications industries.**
- **More than 100 key partners are helping drive development of HyperTransport technology.**

Where can I find HyperTransport™ Technology?

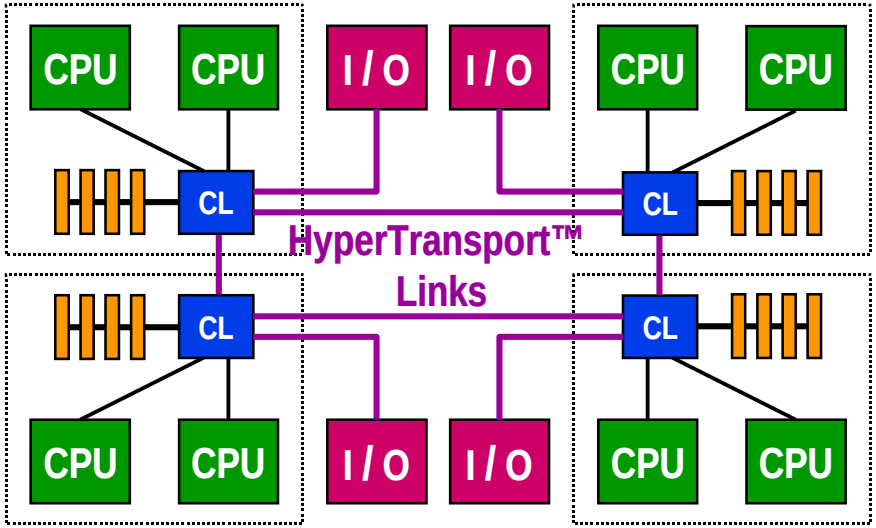
- Routers
- Hubs
- Switches
- Servers
- Workstations
- PCs (Desktop & Notebook)
- Set-Top Boxes
- Mobile/Handheld Devices
- Game Consoles
- Others

HyperTransport™ Technology for Internet Acceleration



Building Block for the Future

- **HyperTransport™ technology is designed to be a building block for enterprise-level server solutions based on AMD's next-generation family of processors**
  - Enables highly scalable multiprocessing systems
  - Designed to significantly increase bandwidth to the "world outside the box"



- **Provides a universal link in servers, workstations and PCs that is designed to help reduce the complexity of system design**

Summary

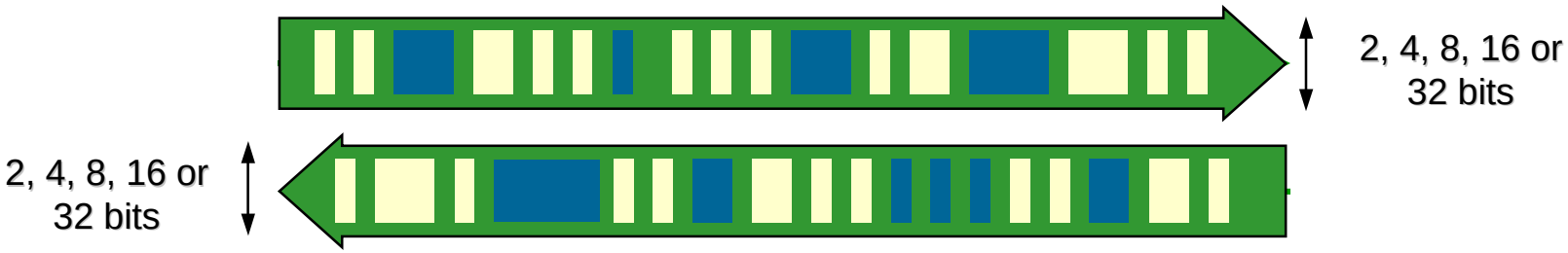
- **AMD's HyperTransport™ technology is an innovative technology that is designed to enable the chips inside of PCs, and networking and communications devices like those that power the Internet, to communicate with each other up to 24 times faster than existing technologies.**
- **HyperTransport technology is designed to increase the speeds at which the components inside of computer and communications devices "talk" with each other, delivering new levels of performance.**
- **AMD is helping drive HyperTransport technology to market through open standards and widespread industry support.**
  - More than 100 partners are helping drive development.
  - Industry heavyweights Broadcom, Cisco Systems, NVIDIA, and Sun Microsystems have all announced plans to use AMD's HyperTransport technology to increase the performance of their future products.
- **AMD plans to use HyperTransport technology to help computers powered by its next-generation family of processors reach new pinnacles of performance.**
- **The first third-party products using AMD's HyperTransport technology are planned to be available later in 2001.**

Backup

HyperTransport™ Technology is designed to provide….

- **a significant increase in I/O bandwidth**
- **a universal link that reduces the number of buses within the system**
- **support for HyperTransport™ technology-based tunnel devices that act as I/O building blocks**
- **a high performance bus for embedded applications**
- **a building block for highly scalable multiprocessing systems**

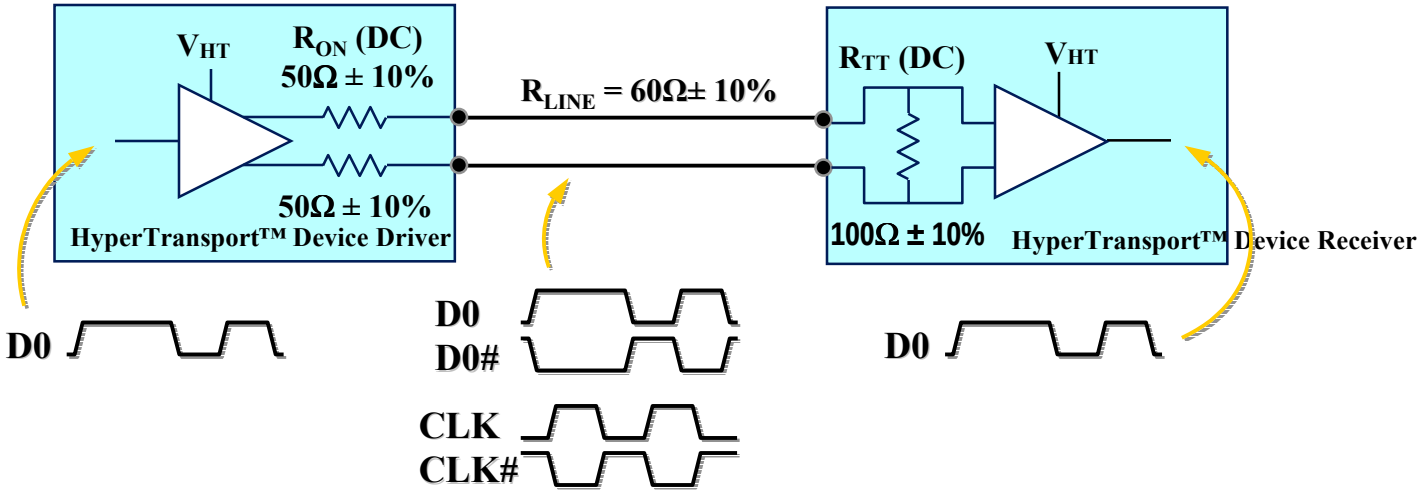
HyperTransport™ Link Basics



- **HyperTransport™ link connections have two unidirectional point-to-point links**
  - The links can be 2-, 4-, 8-, 16-, or 32-bits wide in each direction
  - HyperTransport I/O has a data rate of 800 Megabits/second per pin-pair (400MHz clock)
    - ***E.g., 8 bits each way gives 800 MB/sec each way; 1.6 GB/sec aggregate bandwidth****
    - ***E.g., 4 bits each way gives 400 MB/sec each way; 800 MB/sec aggregate bandwidth****
  - For multiprocessing the CPU-to-CPU link data rate increases to 1.6 Gbits/second
    - ***E.g., 16 bits each way gives 3.2 GB/sec each way; 6.4 GB/sec aggregate bandwidth****
- **Packets are multiples of 4 bytes in length**
  - On links less than 32 bits, bit times concatenate to achieve the 4-byte granularity
- **Commands, addresses and data use the same bits**
  - Data packets after read responses or writes can be 4 to 64 bytes long

* The sweet spots for HyperTransport™ technology-based device configurations

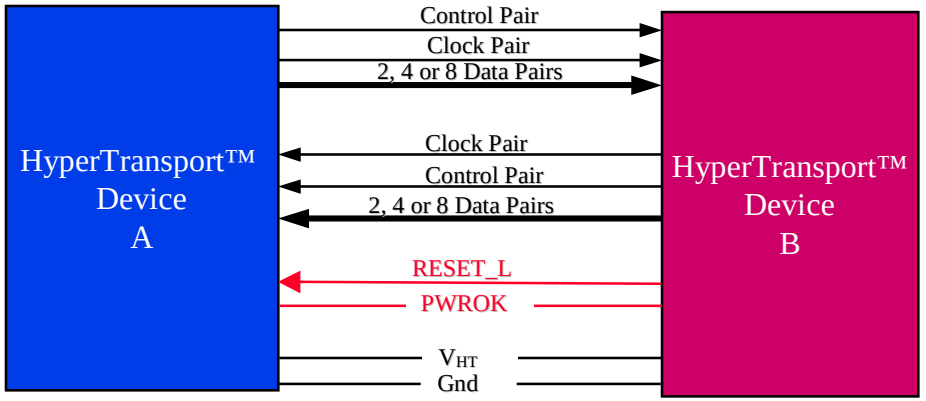
HyperTransport™ Technology Physical Layer



- **Low voltage, differential signaling**
  - Two pins per bit - pin pairs swing in opposite directions
  - V_{HT} is 1.2 volts ± 5% resulting in a differential output of 600 $mV_{TYPICAL}$
  - Differential voltage at the receiver inputs can be as low as 200 mV
- **100 ohm differential impedance for low cost PCBs**
  - No special PCB stack-up should be required
  - Trace lengths up to 24 inches for 800 Mbit/sec operation

HyperTransport™ Device Pin Count

- **Additional HyperTransport™ Device signals**
  - Power OK (PWROK)
  - Reset HyperTransport Device (RESET_L)
- **55-pin HyperTransport device bus provides 12X the bandwidth of PCI-32/33 with fewer pins**
- **Signal to ground ratio is designed to be 4:1**
- **Optional link power down signals for mobile systems**
  - HyperTransport Device Stop_L
  - DevReq_L
- **Power per pin-pair is nil when in HyperTransport Device Stop mode**



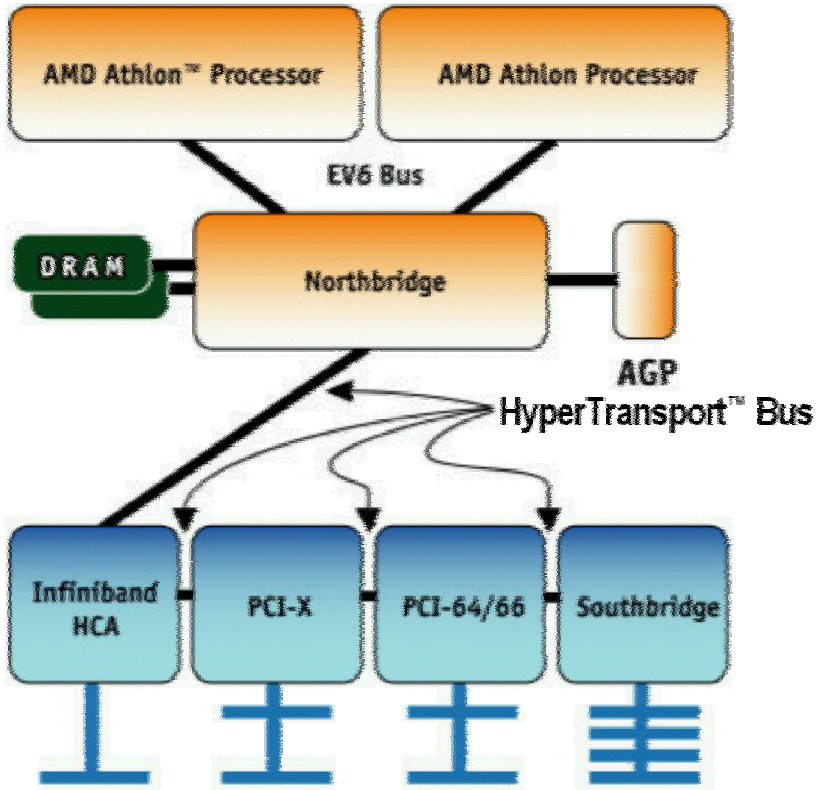
PWROK, RESET_L required for proper reset & init
$V_{HyperTransport}$ routed between devices is required for proper common mode range

Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**

DC Power per Pin-Pair: **4 - 9 mW, 6 $mW_{Typical}$**
Signal to V_{HT}/Gnd Ratio: **4:1**

HyperTransport™ Tunnel Devices

- **HyperTransport™ technology-based I/O is designed to have ample bandwidth to support daisy chained I/O devices.**
  - **Multiple HyperTransport tunnel devices can be daisy chained on a single I/O link.**
  - **HyperTransport bridge devices can be viewed as generic - reusable building blocks for system design.**
- **With HyperTransport tunnels, a basic HyperTransport chipset can be designed for use in server and workstation markets.**



HyperTransport™ Technology Milestones:

- **First public presentation at Microprocessor Forum 99**
- **Operational specification version 1.0 finished in May 2000**
  - 1.01C available now (upon signing a license agreement)
- **Electrical Specs nearing completion**
- **HyperTransport™ Technology presentation with technical information at WinHEC 2000**
  - Great success with about 1,500 participants in our session
- **HyperTransport Technology white paper becomes available early 2000**
- **HyperTransport™ Technology presentation at Platform 2000 (June 2000)**
- **First HyperTransport technology-based south bridge announced by NVIDIA**
- **Sibyte (Broadcom) announced its MIPS cpu with HyperTransport technology**
- **Sandcraft announced its HyperTransport technology roadmap**
- **100+ companies evaluating spec; list is growing**
  - About 4-5 new requests are being received each week
- **First licensees - Others to come soon**
  - Several companies signed; others in the pipeline
  - Numerous other companies have expressed the intention to license HyperTransport technology.
- **Altera first FPGA family in Q1 2001; others to follow**
- **AMD has first silicon samples of a sophisticated south bridge.**
  - PCI boards in house with two chips talking to each other using HyperTransport technology.
- **Multiple HyperTransport technology-based chipsets for AMD Athlon™ processors in 2001**
  - AMD actively working to implement this technology with the core logic partners.
- **InfiniBand solutions are in design now**
- **HyperTransport Technology Consortium planned**
- **HyperTransport technology-based products are planned from AMD in 2002**
  - Partners plan to have products sooner

Cautionary Statement

This presentation contains forward-looking statements, which are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements are generally preceded by words such as “expects”, “plans”, “believes”, “anticipates”, or “intends.” Investors are cautioned that all forward-looking statements in this presentation involve risks and uncertainty that could cause actual results to differ materially from current expectations. Forward-looking statements in this presentation include the risks that AMD will not be able to implement the HyperTransport™ technology in a server or multiprocessor computer system that uses AMD processors; that the HyperTransport technology will not gain widespread industry or market acceptance; that AMD or third parties will not develop and distribute HyperTransport technology-based products in a timely manner, if at all; and that a HyperTransport consortium may not be formed by AMD. We urge investors to review in detail the risks and uncertainties in the company’s Securities and Exchange Commission filings, including the most recently filed Form-10K.